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16. (Twice Amended) A transistor as recited in claim 13, further including a further insulator layer deposited over at least said source and drain regions and planarized to said gate structure.

17. (Twice amended) A transistor as recited in claim 12, wherein said gate structure is between said source and drain regions.

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21. (Twice amended) A transistor as recited in claim 12, wherein said impurities have been supplied by diffusion from a sidewall formed of a doped material and located in said trench.

REMARKS

Claims 12 - 21 remain active in this application. Claims 1 - 11 and 22 have previously been canceled. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 12 and 15 - 17 have been amended to improve form and descriptiveness (to clarify that the recited trench or the patterned dielectric material in which the trench is formed may not be present in the completed transistor, as recited in claim 13). Support for the amendments of the claims is found throughout the application, particularly in Figure 10 and the description thereof on page 14 as well as on pages 11 and 12 and claim 13 of the application as originally filed. No new matter has been introduced into the application.

The Examiner indicates a change should be made in claim 17 for proper antecedent language correspondence. The suggested change has been made in the above amendment. Therefore, to the extent that the Examiner's comment may be a requirement, objection or rejection, it is respectfully submitted that a full

response rendering such requirement, objection or rejection moot has been made.

Claims 12 - 21 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite, the Examiner criticizing claims 12, 13, 15, 16, 20 and 21 (the reference to claim 1 being assumed to be an intended reference to claim 12). This ground of rejection is respectfully traversed, particularly as being moot in view of the amendments made above.

Specifically, in claim 12, "precisely desired location" has been changed to "a location precisely *defined* by said edges of said trench" (emphasis added). In regard to claims 15 and 16, it is respectfully submitted that there is no possible ambiguity between the recited insulator layers in view of the respective recited locations thereof. However, in an effort to expeditiously resolve the issue, the insulator layers are distinguished by recitation that the insulator layer over the source, drain and gate structure is a "further" insulator layer.

In regard to claims 13, 15 -16 and 20 - 21, the Examiner's criticisms appear to be based on an asserted contradiction between the claims in regard to structures used in fabrication of the transistor which do not remain in the completed transistor. It is respectfully submitted that these criticized recitations, in context, are proper structural definitions of the device. For example, in regard to claim 21, the use of a sidewall in a trench as a diffusion source for impurities will cause the impurity concentration to have a characteristic distribution specific to the geometry of the interface of the material into which diffusion occurs and thus is a proper recitation of a feature of the structure in accordance with the invention. Similarly, in regard to claims 12 and 13, registration between the impurity location and the gate edges is assured by use of a

common trench for formation of both structures regardless of whether or not the original trench is removed and replaced or allowed to remain in the transistor; both possibilities being fully disclosed in the original specification at page 11. By the same token in regard to claim 20, page 16, lines 6 - 8, recite the removal of the spacer permissively (i.e. that the spacer may be allowed to remain in the transistor, if desired. Likewise, it is respectfully submitted that the Examiner is incorrect in asserting that planarization contradicts deposition of material on the gate structure. On the contrary, deposition of material on the gate structure or any other structure or surface is commonly a condition precedent to planarization of that material to the recited structure or surface.

Nevertheless, it is respectfully submitted that the Examiner's criticism of claim 13 has been rendered moot by the clarifying amendment to claim 12, claim 16 has been revised, including dependency, to avoid any possibility of contradiction of claim 15 and claim 21 has been revised to improve form in regard to antecedent language and to avoid any inference of recitation of a sidewall remaining in the completed device.

Accordingly, it is respectfully submitted that the Examiner's criticisms are in error and certainly no longer tenable. Therefore, reconsideration and withdrawal of the same is respectfully requested.

Claims 12 - 14 and 17 - 21 have been rejected under 35U.S.C. §102 as being anticipated by Nowak et al.; claims 12 - 14, 17 and 19 -21 have been rejected under 35 U.S.C. §102 as being anticipated by Long et al.; claims 15 - 16 have been rejected under 35 U.S.C. §103 as being unpatentable over Nowak et al. in view of Lee; and claims 16, 16 and 18 have been rejected under 35 U.S.C. §103 as being unpatentable over Long et al.

in view of Lee. These grounds of rejection are respectfully traversed.

While the Examiner is correct in asserting that product-by-process claims are directed to the product and that a product having the same features answers the claims regardless of how the product is actually made, it is respectfully submitted that the transistor structures of Nowak et al. and Long et al. do not have the features explicitly recited in the claims and the deficiencies in the teachings and/or suggestions thereof to answer the claims are not remedied by the teachings and/or suggestions of Lee. Further, while the process may be ultimately unimportant to a determination of patentability of a product, it is respectfully submitted to be improper to totally ignore the respective processes of the invention and the reference(s), as the Examiner has done, since the respective processes are clearly probative of the threshold and underlying question of whether or not the products are the same or substantially similar, particularly where, as here, claim recitations such as the trench may substantively be *either* a process or a structural recitation. It is well-settled that the Examiner must establish at least arguable substantial similarity of products to shift the burden of demonstrating a difference to the Applicant. In other words, if a (possibly) process recitation in a product claim produces a beneficial effect not available from other processes (e.g. the process of a reference), substantial similarity of the products has not been established to shift the burden of showing a difference (absent consideration of the process, itself) in the product to the Applicant. Therefore, consideration of the respective processes for the purpose of determining whether or not the products are the same or similar is respectfully submitted to be not only proper but obligatory. Moreover, it is respectfully submitted

that the Examiner's observations regarding at least Nowak et al. are largely incorrect.

Specifically, the Examiner asserts that Nowak et al. teaches precisely located impurity regions at edges of a trench defined by dielectric 35. However, it can be readily appreciated from Figures 1D and 1F of Nowak et al. and the paragraph bridging columns 2 and 3 that the implantation is performed using mask 19 well before dielectric 35 is formed and, moreover, the implantation(s) are performed over a relatively broad region of the transistor largely coextensive with the source and drain regions and through layers of material (which would reduce accuracy of implant location) rather than a precisely defined location, and particularly not *adjacent* to the source and/or drain regions. Mask 19 provides only a single edge, much in the nature of a block-out mask and the implant region is thus necessarily not smaller or more accurately located than the resolution accuracy of the lithography tool.

More specifically, one implantation of Nowak et al. forms a region 21 which functions as a low-resistance connection (column 3, lines 6 - 8) while the other implant provides damage (for enhanced hole-electron pair production to create a connection from the floating body to the source, much in the manner described in the "Background" section of the present application on page 4, line 23+, over tub region 24 while only the inner region 23 thereof is operative for such function (column 3, lines 20- 25). That is, while region 23 appears well-defined in Figure 1D *et seq.*, the implantation which produces the hot electron generation enhancement at that location extends throughout region 24 which is even more extensive than region 21. Therefore, it is clear that Nowak et al. does not provide impurities in a precisely defined location adjacent the source and/or drain region much

less by virtue of a trench in combination with a gate formed in the same trench. Thus, it is seen that Nowak et al. is not even arguably similar to the invention claimed so as to shift the burden of demonstrating a difference to Applicant and, moreover, the invention has been distinguished from prior art similar to Nowak et al. (e.g. using a source connection approach to reducing floating body effects) in the original application papers.

Therefore, due to the Examiner's substantive error in regard to the teachings of Nowak et al. and the improper analysis of the claimed subject matter relative to Nowak et al., it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of anticipation (or obviousness), based on Nowak et al. of the subject matter of any claim in the application or, even more fundamentally, has not made a *prima facie* demonstration of substantial similarity of the product of Nowak et al. to the claimed product.

The same errors are evident in the rejection based on Long et al. except that the statement of the rejection is devoid of any reference to a trench for either location of an impurity implant or formation of a gate, as claimed, being taught by Long et al. On the contrary, Long et al. uses a raised gate structure with spacers and an angled implantation to produce asymmetrical diodes which, as also discussed in the present application at page 4, lines 6 - 22, restricts design flexibility and tailoring of diode characteristics due to low accuracy of impurity structure placement and coupling of the source and drain implant processes, limiting available transistor performance even while requiring increased process complexity. Since the invention has been distinguished from prior art similar to Long et al. in the original application papers, the Examiner has not made a *prima*

facie demonstration of substantial similarity of the products, much less a *prima facie* demonstration of anticipation (or obviousness) based on Long et al. of the subject matter of any claim in the application.

Lee is cited by the Examiner for the limited purpose of teaching deposition of an insulator layer and planarization to the gate structure. Lee also appears to form the gate structure in a trench (and sidewalls therein) which also serves as an implant mask but does not teach or suggest supplying impurities to the substrate at locations precisely defined by edges of the trench to achieve asymmetrical diode characteristics. Therefore, lee does not supplement the teachings or suggestions of Nowak et al. or Long et al. in regard to the deficiencies of those references to answer the claimed subject matter. Therefore, it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of obviousness of any claim in the application based on the combination of Nowak et al. or Long et al. and Lee.

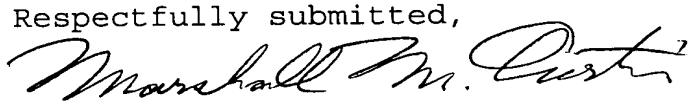
Accordingly, it is respectfully submitted that all of the rejections based on prior art are in error and the Examiner has failed to make a *prima facie* demonstration of the propriety of any asserted ground of rejection. Moreover, the Examiner has not properly evaluated either the subject matter of the claims or the teachings and suggestions of the references. The references clearly do not provide evidence of a level of ordinary skill in the art which would support a conclusion of anticipation (e.g. through inherency) or obviousness) since they do not achieve or lead to an expectation of success in achieving precise impurity structure location and gate alignment therewith allowing improved electrical performance and characteristics at reduced size while reducing process complexity. Therefore it is respectfully requested that the rejections based upon prior art be

reconsidered and withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to International Business Machines Corporation Deposit Account No. 09-0458.

Respectfully submitted,



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APPENDIX

Page 3, line 8+:

To do so, the diode junctions must be made somewhat leaky to allow the floating body of the transistor to be discharged to an acceptable degree. Unfortunately, since field effect transistors are generally formed symmetrically with identical source and drain impurity structures, development of such a characteristic reduces the ratio of resistance of the "on" and "off" states of the transistor, often referred to as the on/off ratio. A large on/off ratio is desirable to support maximum circuit fanout (the number of transistor gates[,] a transistor can drive with acceptable switching speed) and to provide maximum signal voltage swing close to the power supply voltage. Therefore, there is a trade-off between limitation of floating body effects and maintaining a suitable on/off ratio.

Page 4, line 6+:

These approaches use angled implants which are asymmetrically placed due to shadowing by a (possibly dummy) gate structure and are largely characterized by substantial process complexity and diffusion of impurities over substantial distances which prevents the formation of sharp impurity concentration gradients and <u>results in</u> low precision of impurity structure placement. The proposed processes also do not provide for differences in impurity concentration between the source and drain but only differences in location. In summary, while some asymmetry is provided, the flexibility of design parameters in accordance with the proposed processes is very limited and, while source and drain characteristics may be made to differ somewhat, the diode characteristics cannot be accurately tailored or independently fabricated.

Page 7, line 14+:

In order to accomplish these and other objects of the invention, a method of forming an asymmetric field effect transistor to control floating body effect and a transistor having reduced or [eliminatde] eliminated floating body effects formed by such a process is provided wherein the method or process includes steps of defining a gate location with a trench in a dielectric layer on a semiconductor layer, supplying impurities to the semiconductor layer at edges of the trench and adjacent source and drain regions, and forming a gate structure on the semiconductor layer in the trench. The impurities are supplied by angled implantation and/or diffusion from a doped solid body formed in the trench to accurately locate desired impurities such that diffusion is not required to drive the impurities to a desired location; thus supporting steep [inpurity] impurity concentration gradients and high performance.

Claims 12, 15 - 17 and 21:

12. (Twice amended) An asymmetric field effect transistor comprising:

[a trench in a dielectric layer on] a semiconductor layer, said semiconductor layer including impurities supplied thereto at edges of [said] a trench in a dielectric layer on said semiconductor layer and adjacent source and drain regions, wherein the impurities have a [precisely desired] location precisely defined by said edges of said trench to produce asymmetrical diode properties at said source and drain regions for reducing floating body effects, said semiconductor layer being formed on an insulator layer, and

a gate structure formed on said semiconductor layer in said trench[, with asymmetrical diode properties at the source and drain regions,

wherein the transistor is substantially free of floating body effects].

15. (Twice Amended) a transistor as recited in claim 13, including [an] a further insulator layer deposited over said source and drain regions and said gate structure.

16. (Twice Amended) A transistor as recited in claim [15] 13, further including [wherein the] a further insulator layer [is] deposited over at least said source and drain regions and planarized to said gate structure.

17. (Twice amended) A transistor as recited in claim 12, wherein said gate structure is between said source and drain [impurity] regions.

21. (Twice amended) A transistor as recited in claim 12, wherein [said sidewall is a doped material and] said impurities have been supplied by diffusion from [said] a sidewall formed of a doped material and located in said trench.